Design Mitigations on Pixel and Column ADC for 1 MGy TID and SEE Tolerant CIS

I. Hafizh[1], P. Santos[1], P. Leroux[1], G. Meynants[1], J. Van Rethy[2], Y. Cao[2]
[1]KU Leuven, ADVISE research group, Geel, Belgium
{idham.hafizh, pedronuno.teixeiradossantos, paul.leroux, guy.meynants}@kuleuven.be
[2]Magics Technologies, Geel, Belgium
{jelle.vanrethy, ying.cao} @magics.tech

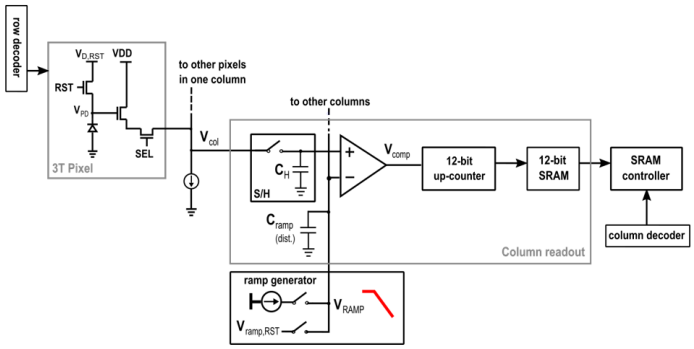
***Abstract*—This article proposes a new pixel and column ADC with radiation-hardened-by-design mitigations for a CMOS image sensor (CIS) to withstand 1 MGy total ionizing dose (TID) and various single event effects (SEE). The pixel consists of a partially pinned photodiode structure combined with butterfly and dog-bone pixel transistors. The p+ layer from the 'pinning' implant, in combination with the shallow trench isolation (STI) structure that is recessed from the photodiode region, prevents the photodiode to collect dark current contributions from TID-induced traps at the Si/SiO_2 interface and shields the photodiode from TID-induced positive charges in the SiO_2. The column ADC employs dual sample and hold stages, dual comparators, and dual 10-bit ripple counters, and utilizes only a single-slope conversion cycle. Each comparator performs double sampling to eliminate comparator offset, which is expected to worsen with TID-induced voltage shift and mismatch. Single-event effects on its counters, i.e. single event upset and transient propagations, are also mitigated by strategic placements of interlocked cell (DICE) latches, buffers, and C-elements. The pixel has a 5µm pitch and the column readout fits in a 10µm pitch, designed in 180nm technology. Preliminary results show limited degradation of dynamic range after TID above 1MGy and high temperature annealing (HTA)**

***Index Terms*—CMOS image sensor, radiation tolerant, TID, SEE, RHBD, pixel, 3T, column ADC, ripple counter**

I. Introduction

A radiation tolerant CIS is increasingly required in many applications in space, scientific research, and nuclear facilities. The main use cases of CIS in space, e.g. celestial body tracker, satellite attitude control, and earth observation, necessitate high radiation tolerance requirement as there is no possibility for camera replacement in case of damage. Cameras placed in large physics experiments such as particle accelerators, synchrotrons, and experimental fission or fusion reactors are continuously exposed to various background radiation with high dose rates that can ultimately damage electronic devices. Applications such as robot navigation, remote handling, site monitoring, or decommissioning in the nuclear industry require CIS devices to withstand up to 1 MGy TID to reach a target lifetime operation of 10-20 years, and to minimize radiation exposure to human operators. Therefore, the study of radiation effects in CIS devices and how to mitigate the effects on various building blocks is essential for these critical use cases.

Designing a CIS using a 180nm technology node presents huge challenges due to accumulative TID effects ranging from mobility degradation, threshold voltage shift, and subthreshold device leakage [1]. The use of special transistor layouts such as annular or enclosed gate layout transistor (ELT), 'dog-bone' [2], or 'butterfly' [1, 3] has been proven useful to eliminate



	Pixel array	Column readout	Peripheral components
TID	• Increased dark current • Voltage level shift due to threshold voltage shift • Increased mismatch (DSNU and PRNU)	• Reduced voltage range due to threshold voltage shift • Leakage on (analog) storage nodes • Increased logic gate delay • Increased mismatch (column FPN)	• Change of ramp slope (ADC gain) or failure • Clock generator frequency shift or failure
SEE	• Bright pixel or blooming due to passing energetic particle • SEU on row addressing	• SEU/SEL and SET on in-column logic, e.g. counter • SEU/SEL on SRAM • SEU/SEL on column addressing	• Ramp disturbance due to SET • Functional interrupt due to SEU/SEL on programming block

Fig. 1. Common 3T CIS architecture with column-parallel readout (top) and identified risks of TID and SEE effects (bottom table)

TID-induced source-to-drain leakage in NMOS devices. However, issues of mobility degradation and threshold voltage shift remain. For example, threshold voltage shift at 1MGy is expected to increase up to 0.15V and 1V for NMOS and PMOS, respectively. Granularity of the TID damage over the chip also suggests a TID-induced mismatch increase between transistors [4]. Besides TID, there are also single event effects (SEE) due to single energetic particle that can induce transient mechanisms such as single event upset (SEU), corrupting a specific frame, or even lasting effects such as single event latch-up (SEL) and single event functional interrupt (SEFI) that can potentially disrupt CIS operation [5]. While detection of energetic particle inside pixel array is unavoidable, SEE can be generally mitigated in circuit level by minimizing the use of latches or registers, e.g. in address decoders, or by implementing classic redundancy strategy such as triple modular redundancy (TMR). However, this strategy is often not feasible to be implemented in the column-parallel readout of CIS due to prohibitive area consumption.

These TID and SEE effects present risks of malfunctions in different parts of the CIS, as summarized in Fig. 1 (bottom). In the following sections, design mitigations for pixel and column ADC in circuit level are presented and compared with previous state-of-the-art.

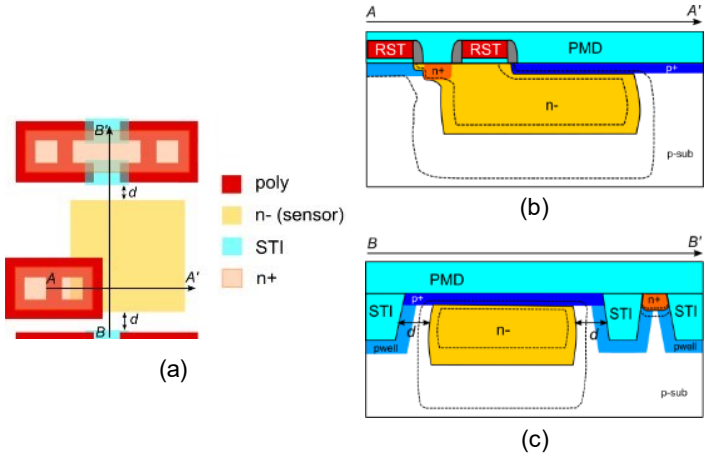


Fig. 2. Proposed radiation tolerant pixel (a), and corresponding cross section along A-A' line (b) and B-B' line (c). p+ implant is applied wherever there is no n+ implant.

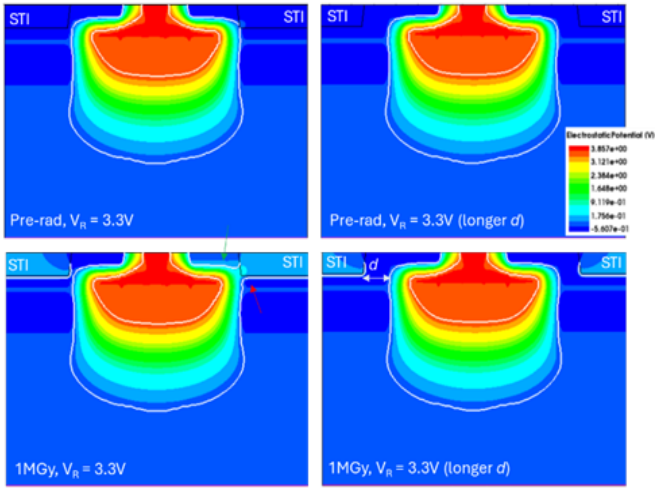


Fig. 3. TCAD simulation results, showing electrostatic potential and depletion region boundaries (white lines) of a partially pinned PD structure. TID effects after 1MGy are modeled by an amount of fixed positive charge and amphoteric traps placed at the Si/SiO2 interface of STI and top oxide surfaces (not shown in this figure)

II. Pixel Design

Radiation tolerant CIS based on 4-transistor (4T) pixel up to TID of 1 kGy for space application has been demonstrated by replacing transfer gate (TG) with an enclosed gate layout, as shown in [6]. However, beyond 10 kGy, the 4T pixels suffer from reduction of charge transfer efficiency and increased image lag, caused by the TID-induced change in potential profile around the pinned PD/TG edge [7]. For higher total dose, with the absence of charge transfer, the 3T pixel is considered to be more radiation tolerant, with the tradeoff of lower performance in pre-rad condition: higher read noise and dark current.

In a regular 3T pixel layout, the STI trench encloses the PD region to prevent crosstalk between neighboring pixels, i.e. photogenerated electrons in one pixel collected by another adjacent pixel. Therefore, along the PD perimeter, the PD junction depletion region always touches the trench, exposing the Si/SiO_2 interface traps located on the STI surface. These traps are the dominant sources of generation dark current. Since the interface trap concentration increases with TID, the PD dark current and its shot noise also increase to an unacceptable level, even up to 6 orders of magnitude at TID ≈ 10 kGy [8]. Several approaches have been demonstrated to mitigate the TID-induced dark current. Instead of using STI, the PD is enclosed by a p+ guard ring [8, 9, 12] or the 'guard' gate placed right on top of a p-well/n- junction to passivate the interface traps [10].

Our approach is described in Fig 2. A p+ implant is placed on top of the n- sensor implant, creating a partially pinned photodiode structure. The p+ layer is used for two purposes: to passivate the interface traps at the pre-metal dielectric (PMD) surface and to form thin depletion region around the p+/n- junction. With the p+ layer, in pre-rad condition, the pixel should achieve lower dark current and higher full well charge per unit area, with the tradeoff of reduced quantum efficiency at the blue wavelength. Besides a p+ implant, for TID-induced dark current mitigation, the STI region is also recessed from the PD region, marked by the distance *d* in Fig. 2a and c. Furthermore, the STI is also passivated by a p-type doping surrounding the trench. This p-well is normally applied on the region outside PD region to tune for NMOS threshold voltage inside the pixel and to prevent crosstalk between pixels.

Fig.3 shows the electrostatic potential of the PD structure under TID effects and various recess distance d as a design variable. From approximately 10 kGy onwards, a depletion region occurs at the edge of the STI. The p-type doping around the STI perimeter ensures that this depletion region remains sufficiently close to the STI. After a high TID level, both charge oxide and interface traps are accumulated on the oxide, leaving the silicon close to the STI and PMD surface depleted. When these new depletion regions touch the photodiode depletion region, very high interface generation dark current will be collected by the PD. The red arrow shows the lateral merging between the PD depletion region and the TID-induced depletion region around STI trenches, which can be avoided by increasing d. The green arrow shows the region under top oxide that remains undepleted, thanks to a thick p+ passivation.

The butterfly and a variant of dog-bone transistors are used for the pixel transistors. The NMOS structure consists of two source and drain n+ wells, each enclosed by the polysilicon gate and p+ well to prevent inter-device leakage. This 'guard' p+ well is then merged with the p+ layer on top of the PD region, creating continuous surface passivation until the edge of the reset transistor. Beyond the partially pinned PD structure, mentioned in [11], and the recessed PD in [12], this work presents a novel combination of a partially pinned PD, the use of butterfly and dog-bone transistors, and the STI passivation by doping and distance control. The combination also allows to fit the PD and three transistors in 5µm pitch, considerably smaller than what is used in previous publications. In this way, the PD depletion region remains isolated in any direction from potential generation dark current sources, except from depletion region under the reset gate.

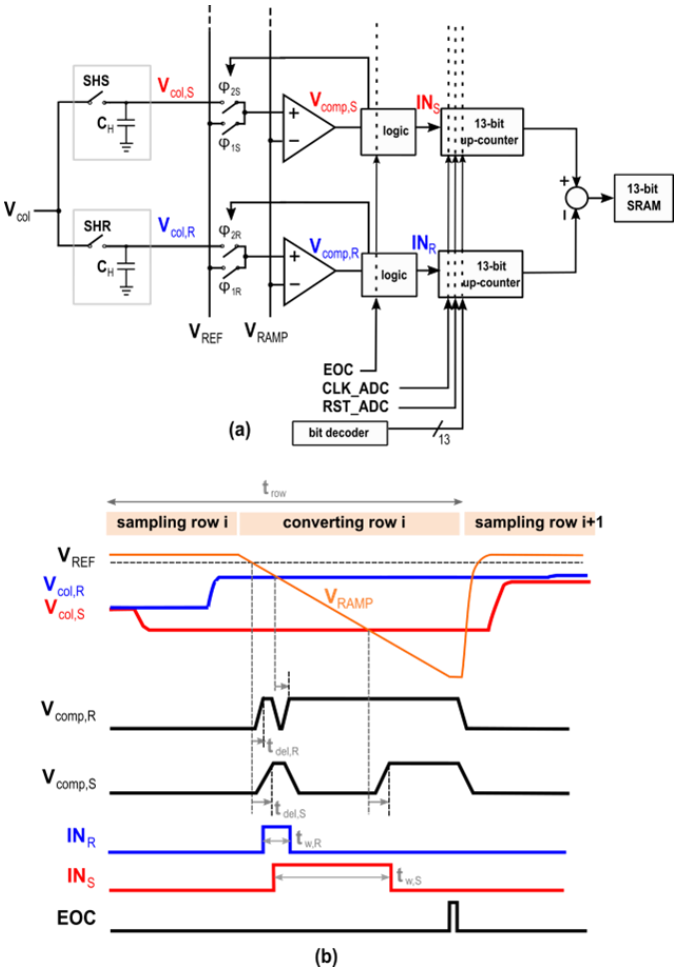


Fig. 4. Proposed radiation tolerant column ADC (a) and corresponding waveforms (b). The counter starts when the comparator toggles the first time and stops when it toggles the second time.

III. Column ADC Design

The most common type of readout in CIS employs a single-slope column ramp ADCs, depicted in Fig. 1 (top). In the best-known circuit topologies, the conversion or ramp cycle is executed twice, to enable digital double sampling (DDS) by subtracting the reset or reference level of the pixel from the signal level. In this proposed ADC shown in Fig. 4a, both reset and signal levels are sampled and converted simultaneously in one cycle using two sample and hold (S/H) blocks, two continuous-time comparators, and two counters in one column readout. With parallel conversion, both levels can be compared against a global single slope ramp. The results of the two counters are then subtracted digitally to get the digital double sampling (DDS) output, to eliminate the offset (and kTC noise, in 4T pixel) introduced by the pixel. The use of a global single slope ramp has several advantages [13]: speed, since it only requires one cycle to complete both conversions, simple ramp generation, and simple timing implementation. Offset or drift on the ramp, which can be caused by TID effect, will also be seen as a common mode disturbance to both signal and reset levels and is therefore inherently eliminated.

The waveforms are shown in Fig. 4b to describe its operation

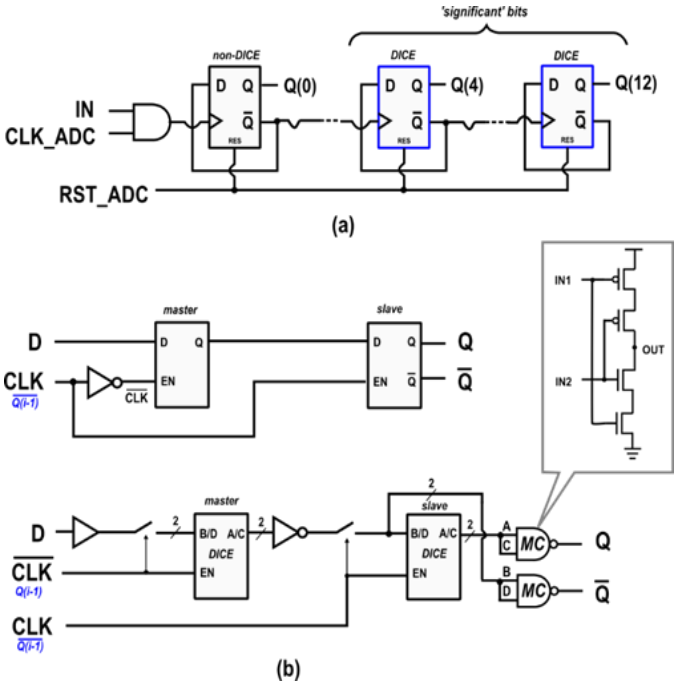


Fig. 5. Radiation tolerant ripple counter (a) and comparison between normal positive edge-triggered master-slave DFF (b, top) and proposed DICE DFF with reduced SEU and SET cross section (b, bottom). MC=Muller C-element.

further. The operation starts with the ramp reset, the reset of the two counters, and both comparators are set in the armed position. Here, a ramp with a negative slope is used. For the first step, the ramp is compared with the common reference level, V_{REF}. This operation will be, in theory, simultaneous in both comparators. However, two comparators will toggle at different times due to the input offset that is reflected as the comparator output delay, $t_{del,R}$ and $t_{del,S}$. While both counters are now running, the comparators are reset and armed again. For the second step, the ramp is compared with the pixel signal (or the pixel reset) level, $V_{col,S}$ (or $V_{col,R}$). Then, the comparator toggles for the second time and stops the respective counter. Since both samples are evaluated by the same comparator, they are affected by the same offset and delay and therefore variations hereon are inherently canceled by the counter operation.

The use of radhard transistors such as annular or butterfly transistors are also selectively used in all blocks, from the S/H stage until the SRAM. After 1 MGy TID, the column voltage is expected to drop up to 0.3V, mainly contributed by the threshold voltage shift of the NMOS 3.3V pixel transistors.

On the digital components, besides using radiation-hardened standard cells, the ripple counter design of the column ADC is also given particular consideration. Ripple counter design is inherently immune to TID, i.e. the TID-induced worsening of the D-flipflop (DFF) propagation delay will not disturb the ripple counter functionality; only a trivial drawback on the output latency. On the other hand, the ripple counter can be very sensitive to single event upset (SEU) or propagating single event transient (SET) on its latches. It can be derived that, if an SEU or SET occurs in the bit i, the ripple counter will result in an addition error by 2^i or 2^{i+1}, respectively. To mitigate this issue, a custom DFF cell in Fig. 5b is equipped with several

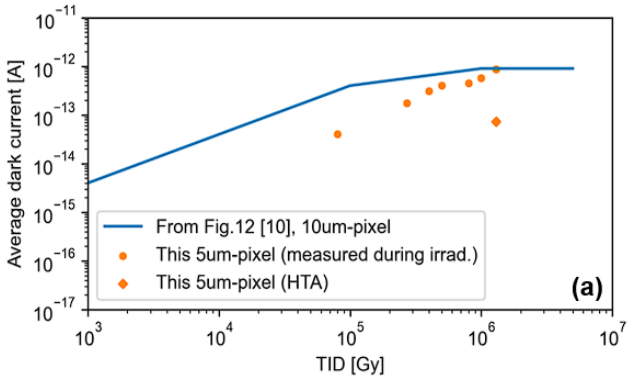


Fig. 6. Measured average dark current estimated from dark frames captured during irradiation and after HTA and the comparison with state-of-the-art radiation tolerant 3T pixel in [10] (a)

features: redundancy based on DICE latches for SEU mitigation [14], and strategic placement of internal buffers, switches, and simplified Muller C-elements [15] inside DFF cells for reducing SET propagation in the ripple counter. This special DFF cells are only placed in a critical part of the column readout such as comparator logic and counter MSBs to maintain efficient area and power consumption, without significant impact on the acquired frame.

IV. CIS Performance vs TID

In the following, the preliminary results of CIS performance measurements before and after 10 keV X-ray irradiation are presented. The sample is irradiated with dose rate = 4.5kGy/h up to 1.3MGy, followed by high temperature annealing (HTA) for 132h at 125°C. While irradiated, the sample was operated at various acquisition modes, and dark frames are also acquired periodically at a fixed exposure time of 10ms. From dark frames, assuming that the rate of charges directly generated by X-ray over time is constant, dark current can be estimated. Comparison between measured dark current from this pixel with the state-of-the-art radiation tolerant 3T pixel [10] are presented in Fig 6a. The proposed 5um-pitch pixel has a lower dark current pre-rad thanks to a smaller pitch and the passivation by p+ surface. During irradiation, which represents accelerated TID damage, the dark current appears to increase at a faster rate compared to pixel reference. However, after HTA, the dark current is reduced by more than an order of magnitude. It is important to note that the data presented in [10] was acquired from different irradiation and measurement conditions, i.e. using higher dose rate and measurements were performed after 24h-7d after X-ray exposure.

In pre-rad condition and after irradiation + HTA, the CIS has also been characterized using the photon transfer curve (PTC) method, where the results are summarized in Table I. The effective full well charge and read noise pre-rad are consistent with the high capacitances contributed by p+/n- junction and gate capacitance of the butterfly transistor. After 1.3MGy TID and HTA, read noise increases due to dark current shot noise and effective full well charge decreases mainly due to V_{TH} shift of NMOS pixel transistor. The combination of read noise increase and full well reduction reduces the dynamic range but still within an acceptable level.

Table I - RadHard CIS Performance

Parameter	Pre-rad	Post-rad 1.3MGy + HTA 125°C 132h
Conversion gain	10.5 µV/e-	8.9 µV/e-
Column voltage range	1.3V	1V
Effective full well charge	125700 e-	94900 e-
Read noise	90 e^-_{RMS}	129 e^-_{RMS}
Dark current	0.06 fA (402 e-/s)	39.5 fA (246.8 ke-/s)
Dynamic range	62.4 dB	57.1 dB

V. Conclusion

The proposed pixel and column ADC withstanding up to 1 MGy TID and single-event effects are presented. The solutions target to minimize the performance degradation, e.g. dark current, effective full well charge, read noise, and dynamic range, during and after operation in an environment with high levels of ionizing radiation. Preliminary results confirm good performance in both pre-rad condition and after 1.3MGy irradiation and high temperature annealing.

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